MityDSP and MityDSP-XM

Board Errata

REVISION HISTORY

Date	Change Description
20-JUN-2011	Initial delivery, added PLLM issue with MityDSPs.
28-JUN-2011	Add serial number information of MityDSPs with the PLL issue
30-JUN-2011	Add serial number information of MityDSP-XMs that potentially have the PLL issue
21-DEC-2012	Added PLL fix PCN information. Added full revision history and links to PCN's for cold start and PLL fixes.

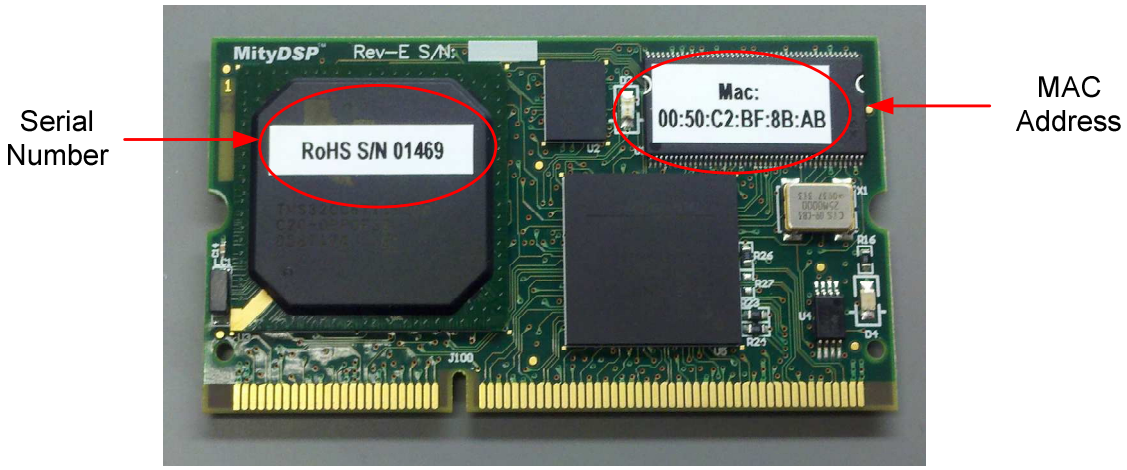
1 Introduction

This document describes any known design issues or exceptions to the functional specifications for the MityDSP 6711 based System On Modules (SOMs) developed by Critical Link LLC.

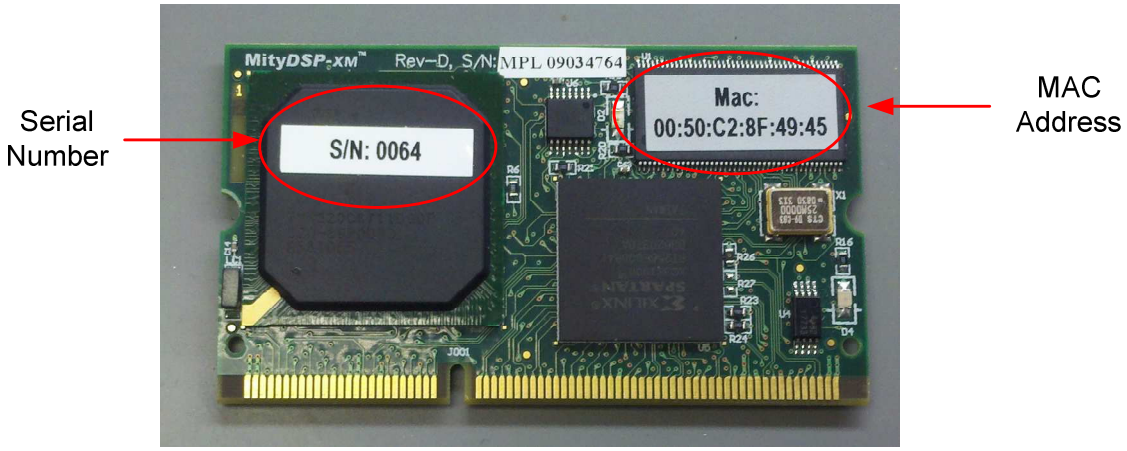
Details regarding the modules may be accessed at http://www.mitydsp.com, and additional support information may be located at support.criticallink.com/redmine/dsp-products.

2 Product Marking

The serial number and MAC address of the MityDSP SOM may be determined by the figure below.



The serial number and MAC address of the MityDSP-XM SOM may be determined by the figure below.



Modules produced after October 2012 also include a label including the Printed Circtuit Assembly (PCA) number, which is of the form “80-XXXXXXXYY-ZZ”. This number

should be used when possible for identification of applicable revision history for an assembly.

3 PCA Product History

The PCA product history for all MityDSP-6711 (legacy MityDSP and MityDSP-XM modules) is listed below. Details for Product Change Notifications (PCNs) may be downloaded from the link below.

Model Number	PCA Number	Applicable Design Exceptions	PCNs
6711-KB-3X3-RI-L 6711-KA-1X1-RI 6711-AA-1X1-RC 6711-AA-1X1-RC-L 6711-AB-3X3-RC 6711-AB-3X3-RC-L	80-000159RI-2 80-000115RI-1E 80-000149RC-1E 80-000174RC-1E 80-000157RC-1D 80-000163RC-1D	- Unstable Operation with PLLM Frequency at 600 MHz - Cold Start Intermittent Failure	
6711-KA-1X1-RI 6711-AA-1X1-RC 6711-AA-1X1-RC-L 6711-AB-3X3-RC	80-000115RI-1E2 80-000149RC-1E2 80-000174RC-1E2 80-000157RC-1D2	- Unstable Operation with PLLM Frequency at 600 MHz	PCN20121221000
6711-KA-1X1-RI 6711-AA-1X1-RC 6711-AA-1X1-RC-L 6711-AB-3X3-RC 6711-AB-3X3-RC-L	80-000115RI-1F 80-000149RI-1F 80-000174RC-1F 80-000157RC-1E 80-000163RC-1E		PCN20121221001

4 Known Design Exceptions and Usage Notes

Usage notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness.

4.1 Cold Start Intermittent Failure

Certain industrial temperature MityDSP and MityDSP-XM modules demonstrated intermittent power-up initialization failures when started at temperatures below -25C.

PCN20121221000 addresses this issue.

4.2 Unstable Operation with PLLM frequency at 600 MHz

MityDSP PCA Number	Serial Numbers Effected
80-000149RC-1 (MityDSP)	1350 through 2147
80-000157RC-1 (MityDSP-XM)	639 through 890

With certain lots of MityDSP and MityDSP-XM modules, it has been observed that the TMS320C6711 processor exhibits apparent instabilities when the phase-locked-loop output signal (PLLsOUT) of the PLL controller block is set to 600 MHz. The PLLOUT signal is used as the fundamental clock for developing the DSP system clocks including the CPU clock, peripheral clocks, and external memory interface (EMIF) clock. Details

of the PLL operation can be viewed in TI's spru233c – Phase-Locked Loop (PLL) Controller Reference Guide.

The default bootstrapper and bootloader software (1st and 2nd stage bootloader software) provided by Critical Link LLC at factory installation configure the PLLOUT signal to 200 MHz and the CPU clock to 100 MHz and EMIF to 50 MHz. Operation of the bootstrapper and bootloader is not affected by this issue.

The MityDSP development kit (MDK), revision 2.2 through 2.9.1 includes a C software header file that provides a C preprocessor macro called RECONFIG_CLOCKS that allows application developers to alter the CPU clock frequency up to 200 MHz. This macro is located in the MDK file "software/inc/core/DspMacros.h" This macro configures the PLLOUT signal to 600 MHz in order to provide a 200, 150, and 100 MHz CPU clock rate option. Applications using this macro may experience instabilities when run on the identified MityDSP SOMs.

To work around the option, two options exist. If the application runs at 100 MHz, do not use the macro on startup. The CPU is preconfigured to run at 100 MHz by the bootstrapper provided by Critical Link. If running at a different frequency than 100 MHz is required, the design engineer should use an updated version of DspMacros.h from MDK version 2.9.2 or higher. This file alters the macro to configure the PLLOUT to 400 MHz. As a consequence, the option for 150 MHz operation is not available.

This header file may be back-ported (i.e., you may overwrite your current version of this file) to previous MDKs if necessary. You do not necessarily need to upgrade your MDK version to apply this work around. A copy of this file is available for download at http://support.criticallink.com/redmine/projects/dsp-products/files. You may need to register for an account for access to the file.

PCN20121221001 addresses this issue with a modification to the PCB hardware.