PCN# 20121221000

Correct Cold Start Intermittent Failure on

MityDSP-6711 Family of System On Modules

Date: December 21,2012
To: Purchasing Agents

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact the Production Manager, Bill Halpin (bill.halpin@criticallink.com).

Sincerely,

Critical Link, LLC
Phone: (315) 425-4045
Fax: (315) 425-4048

PCN Number: 20121221000
PCN Date: December 21, 2012
Title: Correct Cold Start Intermittent Failure on MityDSP-6711
Contact: Bill Halpin
Phone: (315) 425-4045
Ship Date: 03/01/2012

Description of Change
The following components were modified on the MityDSP-6711 and MityDSP-6711 XM modules.

ID	Change From:	Change To:	Reason
D1	BAV99	BAT54S	Temperature Stability
R11	100K Ω	1.00K Ω	Reset Signal Margin
R12	100K Ω	10.0K Ω	Reset Signal Margin
R14	200K Ω	20.0K Ω	Reset Signal Margin
C43	15pF	1000pF	Reset Signal Margin
R4	330 Ω	200 Ω	FPGA Programming Signal Margin
R21	1.00K Ω	200 Ω	FPGA Programming Signal Margin
R22	1.00K Ω	0 Ω	FPGA Programming Signal Margin
R29	330 Ω	200 Ω	FPGA Programming Signal Margin

Reason of Change
There was limited margin on the CCLK signal from the DSP to the FPGA. This signal is required for programming the FPGA. The internal pull-up resistor on the CCLK pin of the FPGA is strong enough to interfere with the V_{IL} detection. The series resistor is too high to pull the signal low with significant margin, so the FPGA programming cycles – part of the initial boot sequence – fail at certain temperature ranges and with specific FPGA production lots. As part of the investigation, several other components were modified in order to increase pull-up or pull-down margins in the reset and FPGA programming circuitry.

Work Arounds
No known work arounds exist for this issue.

Anticipated Impact on Form, Fit, Function (positive / negative)
No impact on form or fit is anticipated with this change.

Anticipated Impact on Quality or Reliability (positive / negative)
Without this change, the industrial temperature rated MityDSPs are likely to experience initialization failures at temperatures between -10°C and -20°C and are highly likely to fail below -39°C. With this change, this failure mode should no longer occur.

Products Affected:
Details regarding the full printed circuit assembly (PCA) revision history can be located in the MityDSP-6711 Errata on the Critical Link support site.

Model Number	Current PCA	New PCA
6711-KA-1X1-RI	80-000115RI-1E	80-000115RI-1E2
6711-KA-1X1-RC	80-000149RC-1E	80-000149RC-1E2
6711-AA-1X1-RC-L	80-000174RC-1E	80-000174RC-1E2
6711-AB-3X3-RC	80-000157RC-1D	80-000157RC-1D2
6711-AB-3X3-RC-L	80-000163RC-1D	80-000163RC-1E