# PCN# 20121203001

# Correct RGMII transmit packet corruption, USB in-rush current, HDMI SDA/SCL pins on

# MityARM-335x Development Kits

Date: December 3, 2012
To: Purchasing Agents

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact the Production Manager, Bill Halpin (bill.halpin@criticallink.com).

Sincerely,

Critical Link, LLC
Phone: (315) 425-4045
Fax: (315) 425-4048

**PCN Number:** 20121203001
**PCN Date:** December 3, 2012
**Title:** Correct Transmit Packet Loss, USB inrush, HDMI DDC lines
**Contact:** Bill Halpin
**Phone:** (315) 425-4045
**Ship Date:** 03/01/2013

## Overview

3 changes to the MityARM-335X development kit printed circuit board are presented below.

## Correct Ethernet Transmit Packet Loss

### Description of Change

The signal termination for the RGMII data lines on the MityARM-335x development kit board has changed from series termination (see Figure 1) to R/C termination (see Figure 2) in order to improve the signal integrity margins and cross talk between the data lines and the RGMII transmit clock and data valid signals. In addition, the TX_CLK line was isolated from the data lines on the PCB layout.

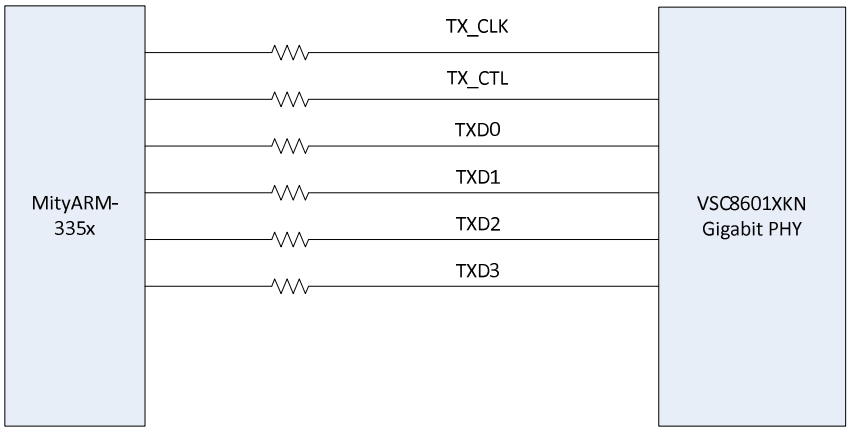


**Figure 1 RGMII Transmit Data Path, Prior to Change**

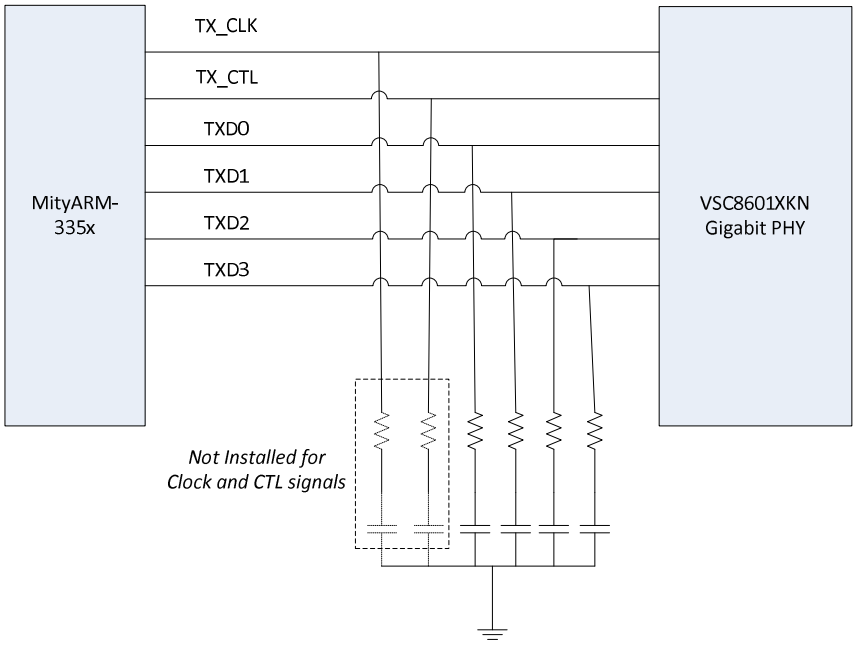


**Figure 2 RGMII Transmit Data Path, After Change**

## Reason for Change

Prior to the change, certain data patterns (for example, a packet containing all "0xF0" octet codes) transmitted from the MityARM-3359 SOM over the RGMII interface to the gigabit Ethernet PHY on the development kit host board could result in packet corruption and failed transmission. The packet corruption was due to signal cross talk to the transmit clock and control lines as well as a small amount of impedance mismatch on the data lines. The data corruption was only observable at low statistical rates when 3 or 4 data lines toggled simultaneously over large packet sizes. Patterns such as 0xF0, which transmitted as nibbles along the RGMII interface resulted in "bit-bang" style data patterns, were used to detect the error condition.

This change resolves the packet corruption, providing the capability to transmit packets without sensitivity to the data payload.

## Anticipated Impact on Form, Fit, Function (positive / negative)

With this change, the successful transmission of long data packets that toggle or "bit-bang" all 4 data lines continuously will be supported.

## Anticipated Impact on Quality or Reliability (positive / negative)

No impact on quality or reliability is expected with this change.

**Correct USB inrush current / Voltage Drop**

**Description of Change**
The bulk capacitance on the VBUS supply pins for the USB 2.0 port connections was increased from 10 microfarads to approximately 120 microfarads.

**Reason for Change**
The USB specification for Host USB devices implies that a minimum bulk capacitance of 120 microfarads should be provided on the VBUS line configurations which share a common VBUS supply with multiple ports. This bulk capacitance should provide enough instantaneous current to support the inrush demands of the worst case USB 2.0 compliant peripheral devices inserted onto the bus.

**Work Arounds**
For boards without the implemented change, a software work-around has been identified that would allow users to (via command) force the USB interfaces to rescan the bus after a device was inserted and the VBUS rail had stabilized. Contact Critical Link for details.

**Anticipated Impact on Form, Fit, Function (positive / negative)**
No change to the specified form, fit, or function of the board is expected.

**Anticipated Impact on Quality or Reliability (positive / negative)**
Without this change, certain USB devices that draw a large amount of current on power up would not properly enumerate when inserted. With this change, identified devices were able to power up and enumerate properly.

**Correct HDMI SDA/SCL Pin Assignments on J400**

**Description of Change**
The DDC Data and Clock lines on J400 were swapped.

**Reason for Change**
The symbol captured for the HDMI connector was consistent with the HDMI video connector specification. The DDC Data and Clock lines had to be reversed in order to be consistent with the specification.

**Anticipated Impact on Form, Fit, Function (positive / negative)**
Because the DDC Data and Clock signals are not electrically connected to the I2C bus of the processor (the level translators that perform this function, Q400 and Q401, are currently not installed), no change to the specified form, fit, or function of the board is expected. However, if in the future Q400 and Q401 are installed, the DDC bus on the HDMI connector is expected to operate within specification.

**Anticipated Impact on Quality or Reliability (positive / negative)**
No impact on quality or reliability is expected with this change.

**Products Affected:**
Details regarding the full printed circuit assembly (PCA) revision history can be located in the MityARM-335x Development Kit Revision History section on the Critical Link support site.

| Current PCA | New PCA |
|---|---|
| 80-000458RI-3A | 80-000458RI-5A3, -5B |