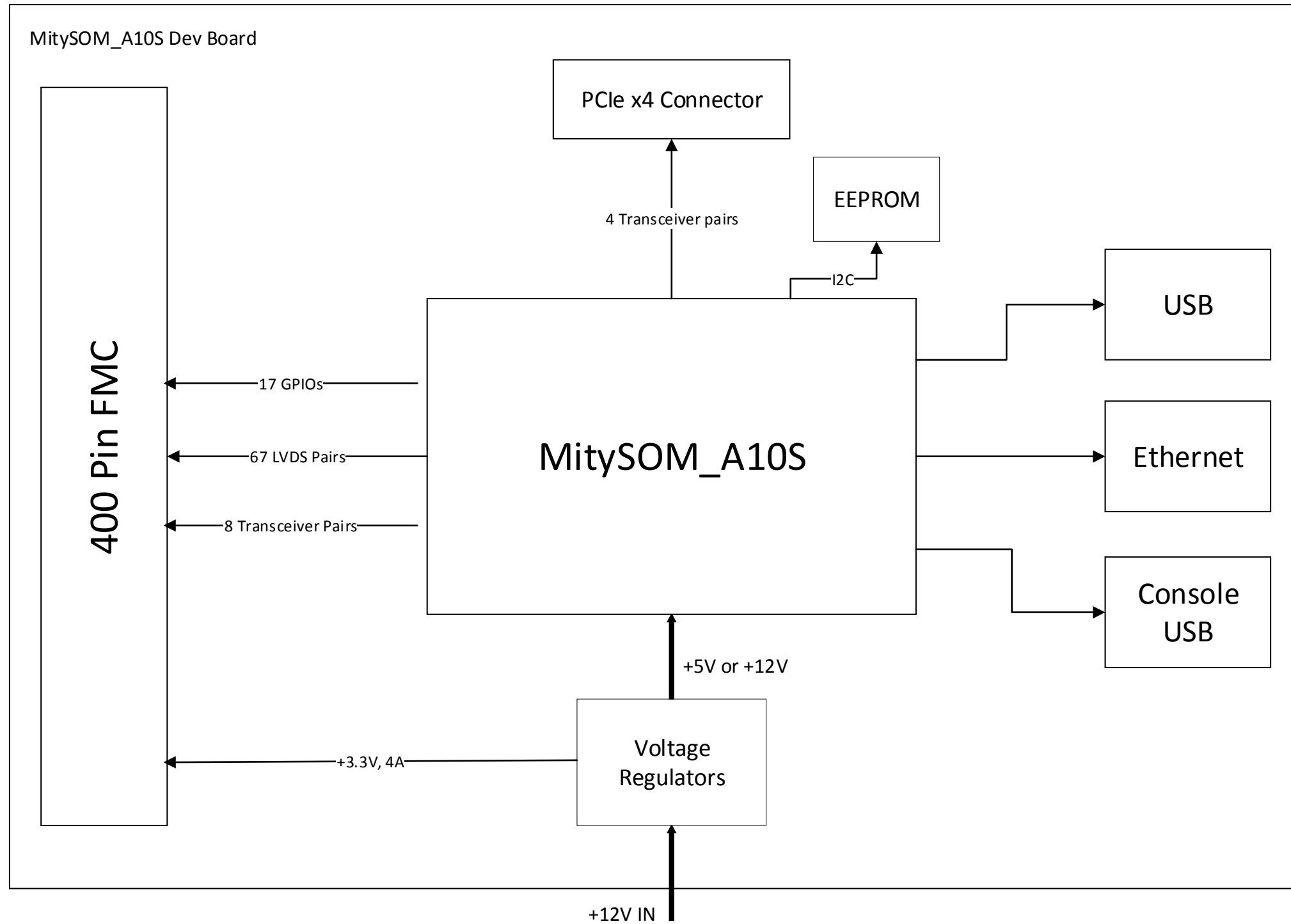


REV	DESCRIPTION	ECR No	INITIALS	DATE
-1A	Initial release	1558	KC	05/07/2018



LBL100  
PCA LABEL  
PCA Label  
80-001127RC-1\_RevA

PCB # 90-000365R-1\_RevA  
PN-PCB100

A

A

B

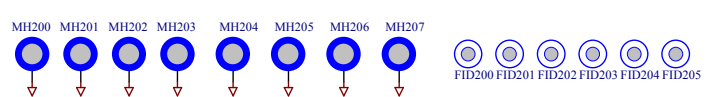
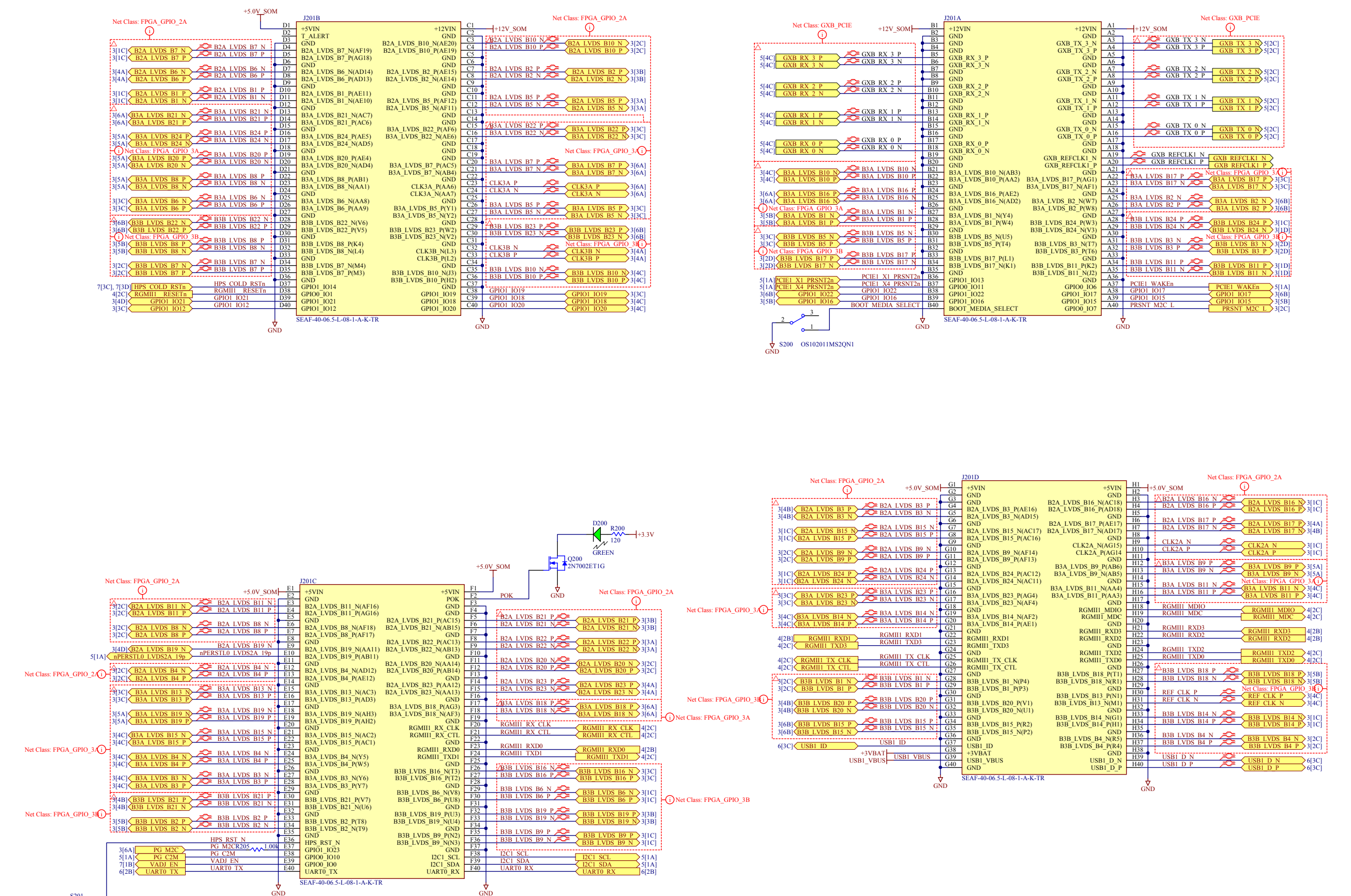
B

C

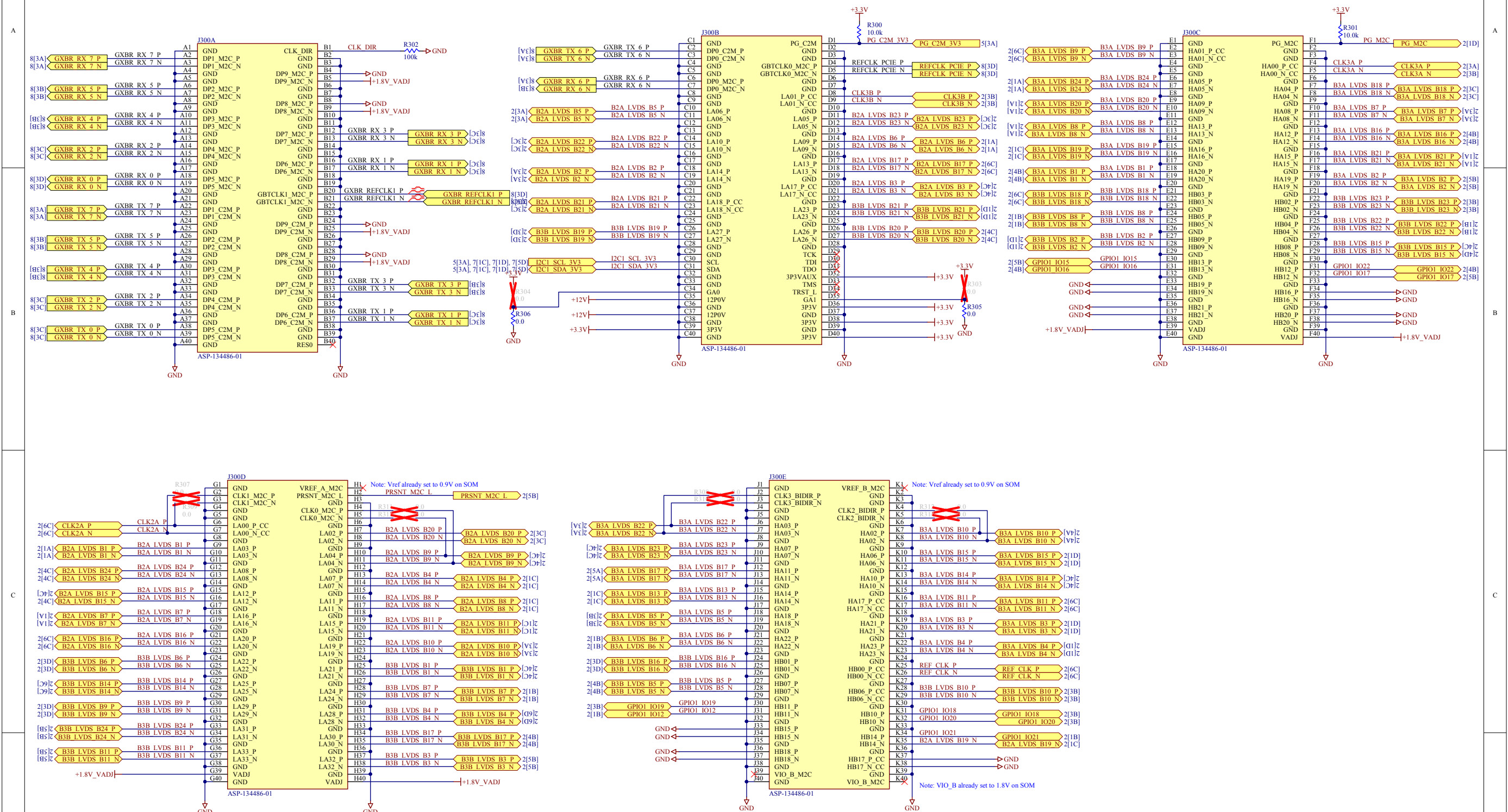
C

D

D

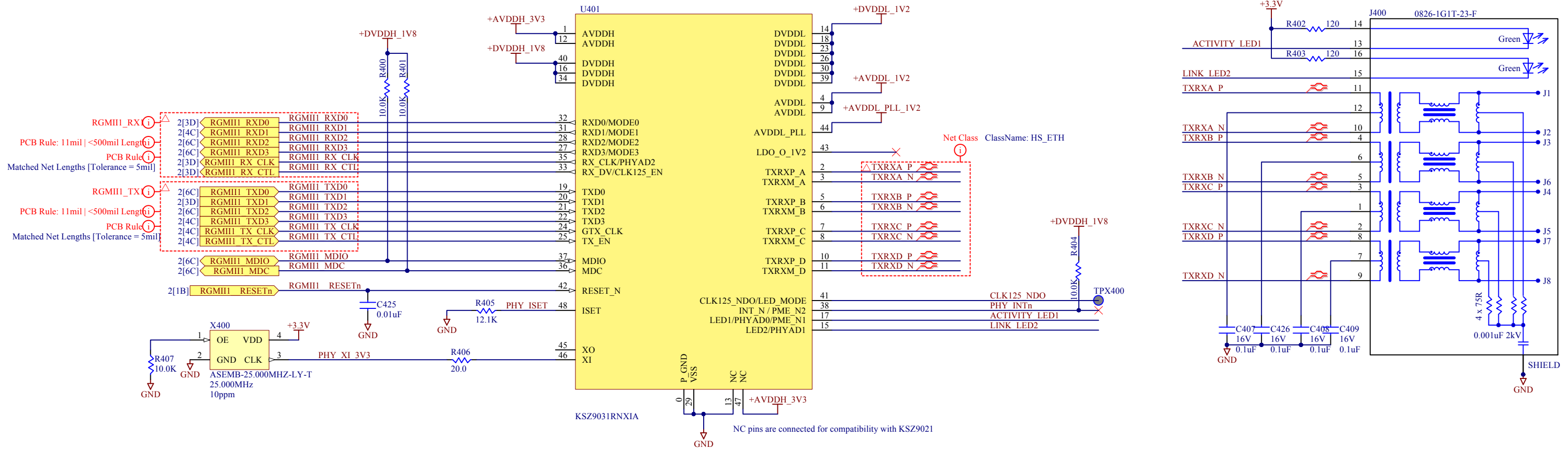
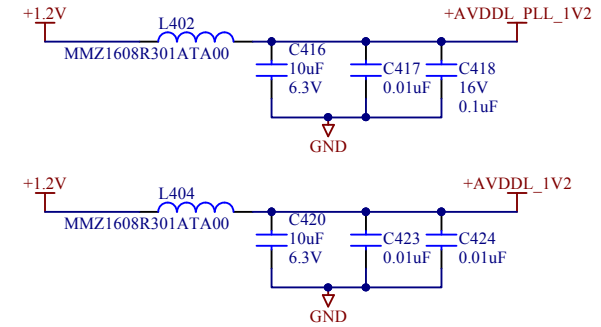
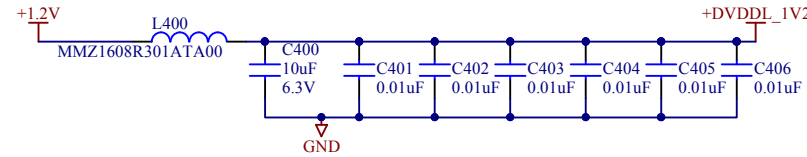
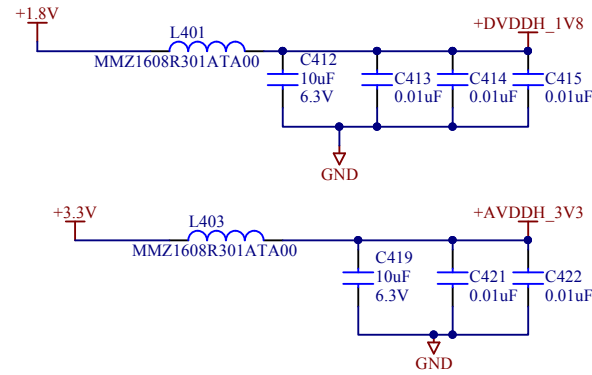


# FMC Connector



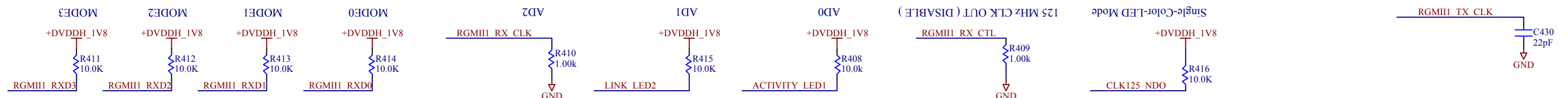
# Ethernet

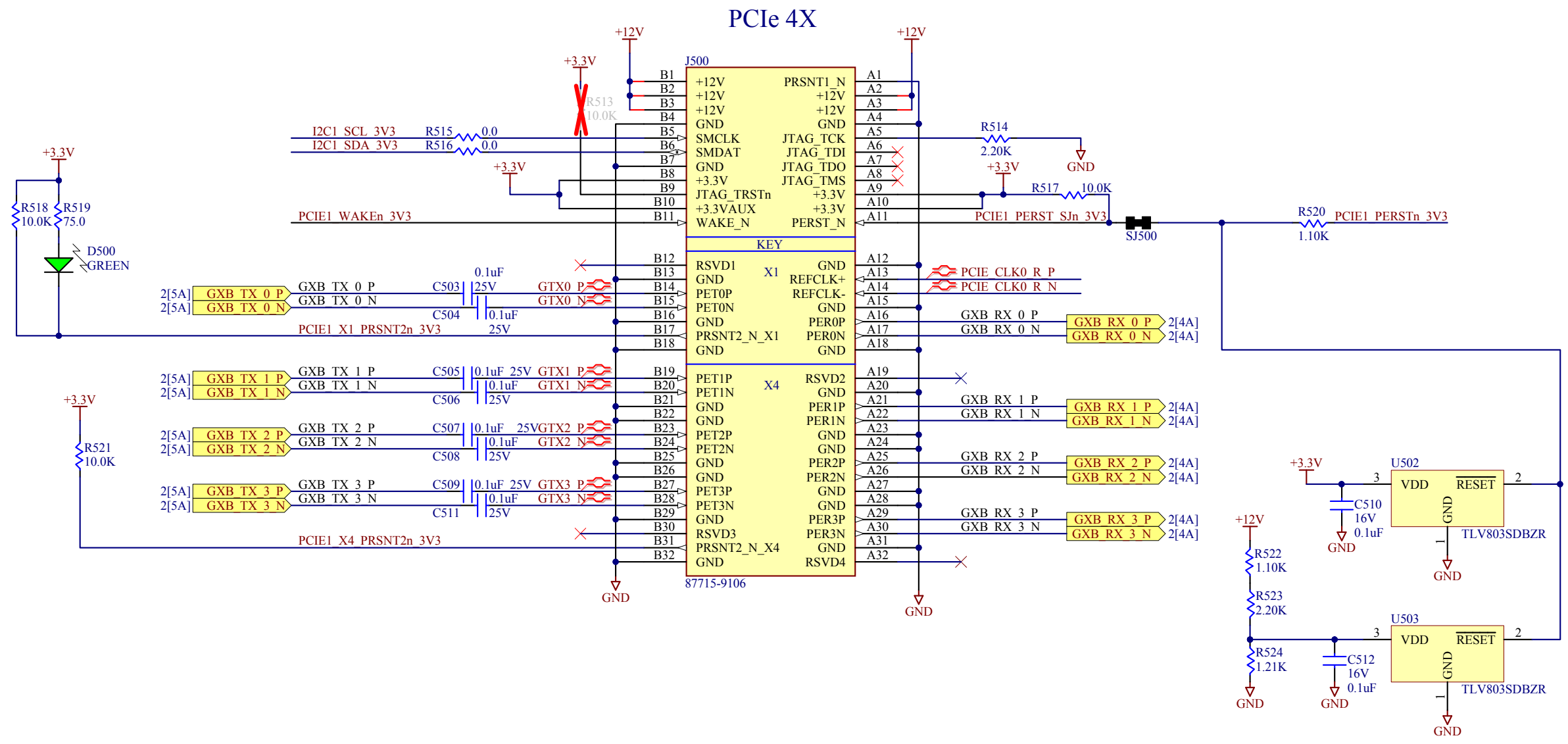
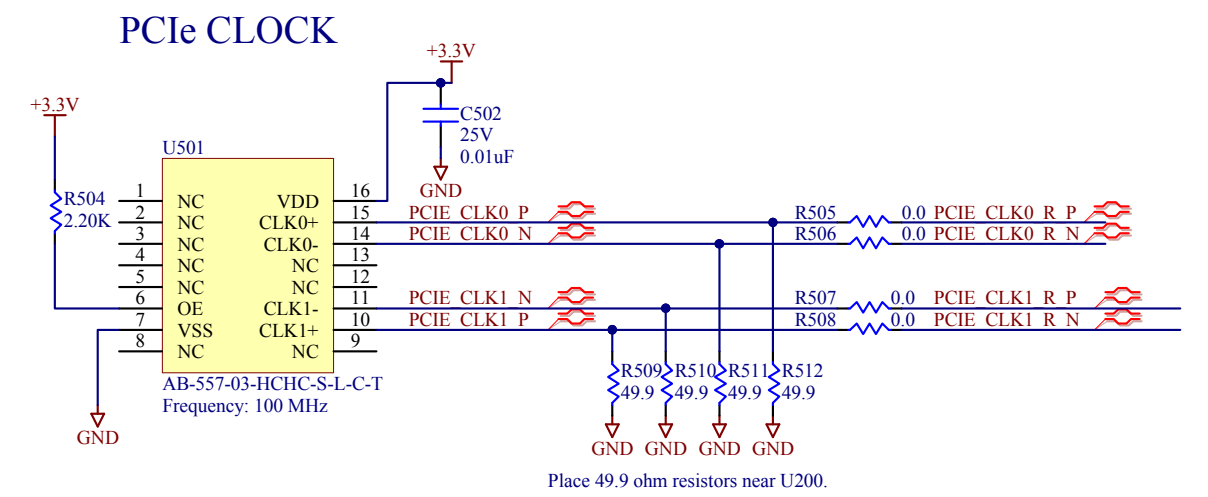
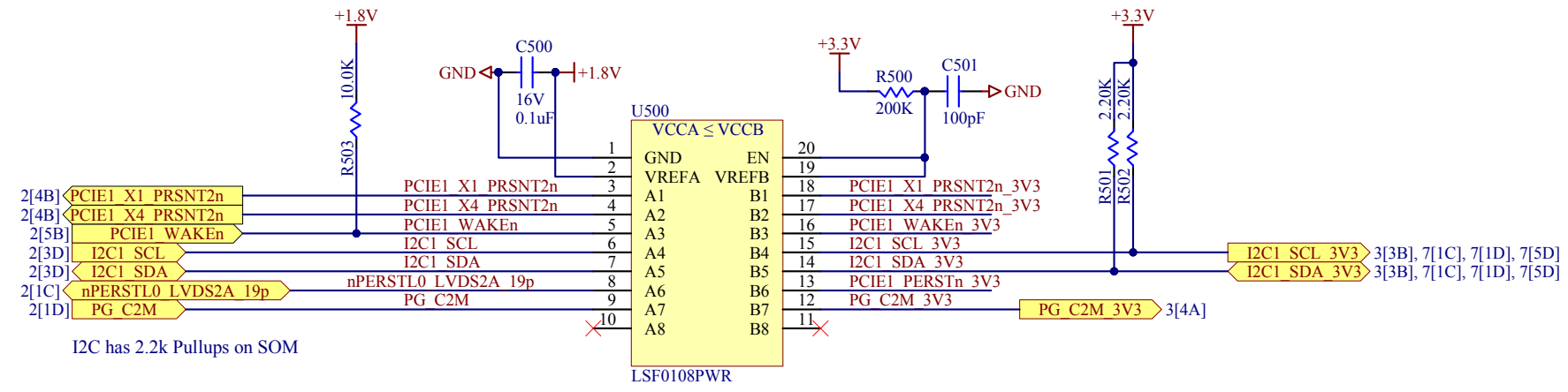
	1.2V Core (DVDDL, AVDDL, AVDDL_PLL) mA	2.5V Transceiver (AVDDH - commercial temp only) mA	3.3V Transceiver (AVDDH) mA	1.8V Digital I/Os (DVDDH) mA	Total Chip Power mW
1000Base-T link-up (no traffic)	210	58.8	67.8	11.2	419 / 494
1000Base-T full-duplex @ 100% utilization	221	57.9	66.3	23.6	452 / 526
100Base-TX link-up (no traffic)	63.6	24.9	28.7	8.4	154 / 186
100Base-TX full-duplex @ 100% utilization	63.8	24.9	28.6	9.8	156 / 189



PHY Mode (Default: 1111): Advertise all capabilities

PHY Address (00XXX, Default: 00011)





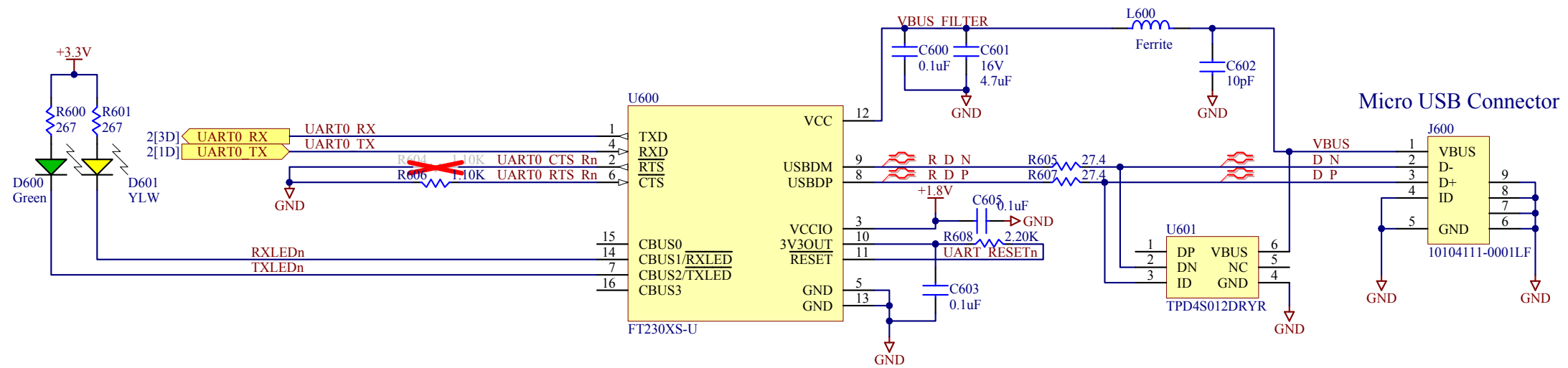
Remove R505,R506,R507,R508 and populate R525 and R526 to convert to endpoint mode from root port

~~PCIE CLK0 R P R525~~ PCIE CLK1 R P  
~~PCIE CLK0 R N R526~~ PCIE CLK1 R N

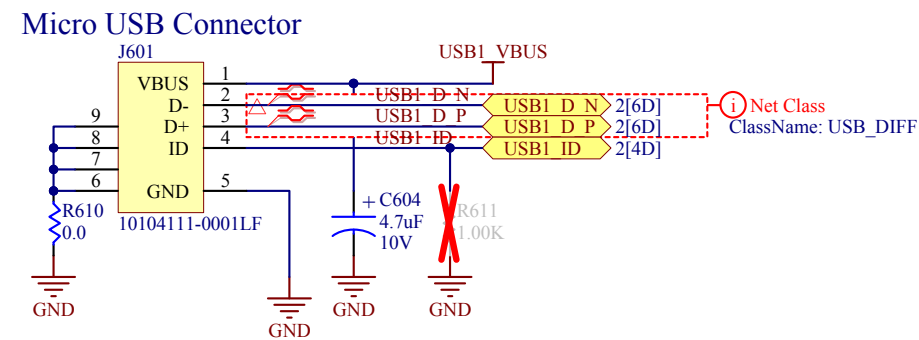
Title: <b>PCIe</b>		Critical Link, LLC 6712 Brooklawn Parkway Syracuse, NY 13211 315.425.4045 www.criticallink.com	
Size: B	Number: 80-001127RC-1	Revision: A	
Date: 5/7/2018	Time: 11:38:34 PM	Sheet 5 of 8	
SVN: 3700	File: PCIe.SchDoc		



## USB to Serial Interface

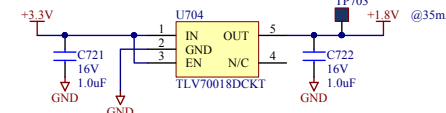
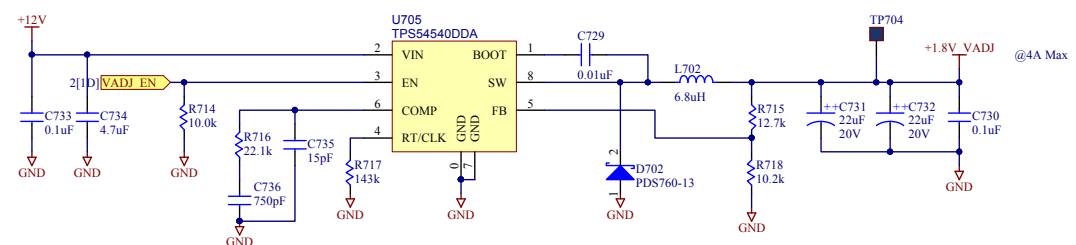
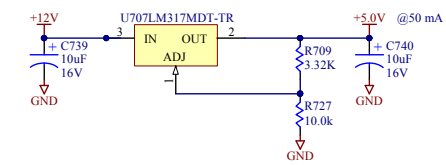
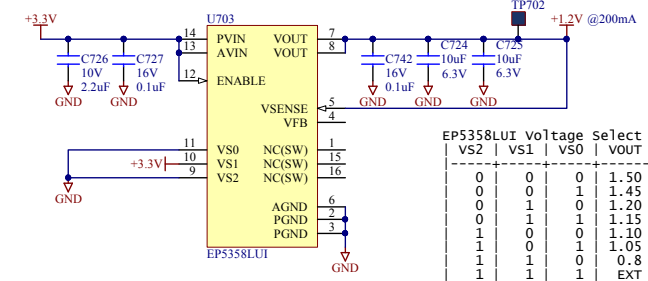
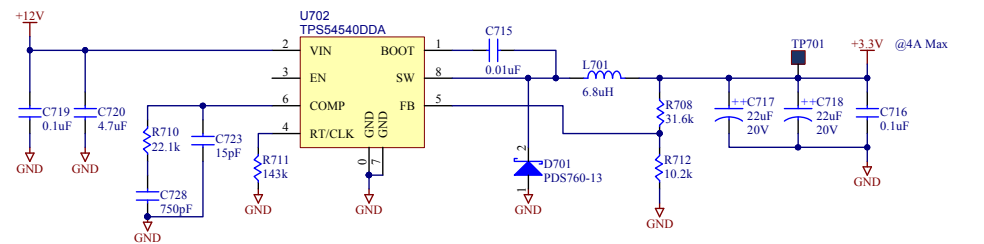
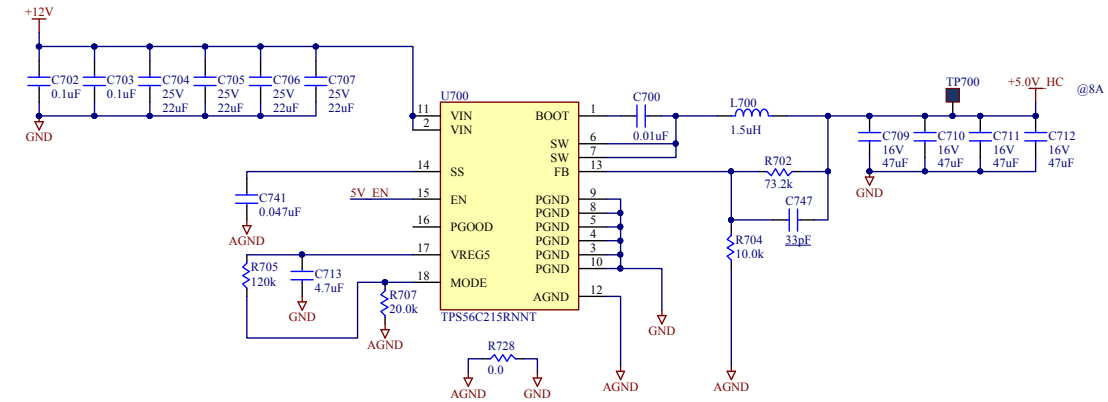
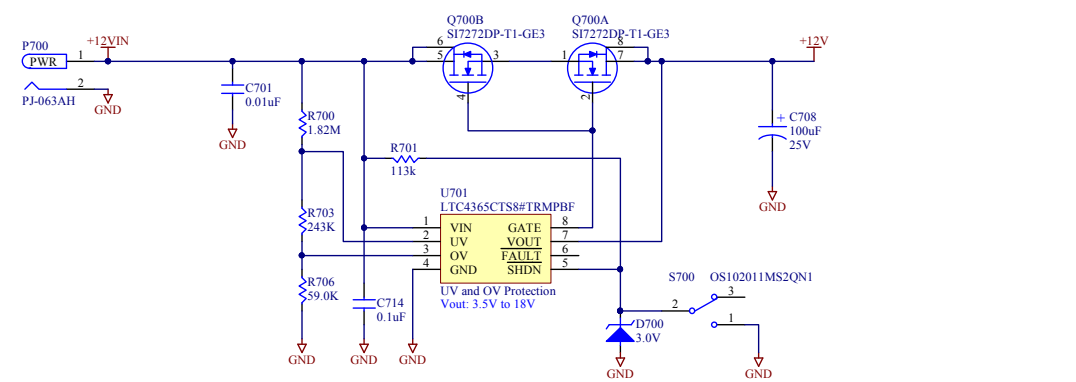


## USB OTG from SOM

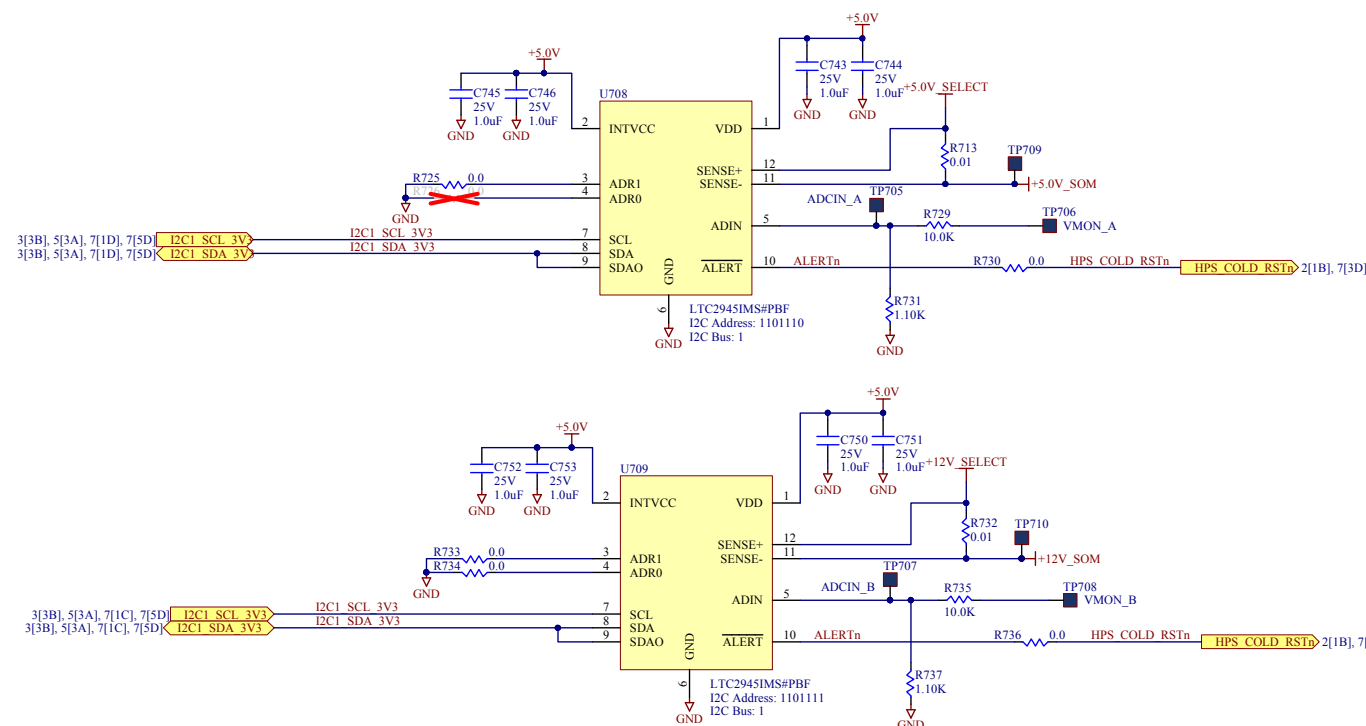


Note: Overcurrent protection provided on SOM

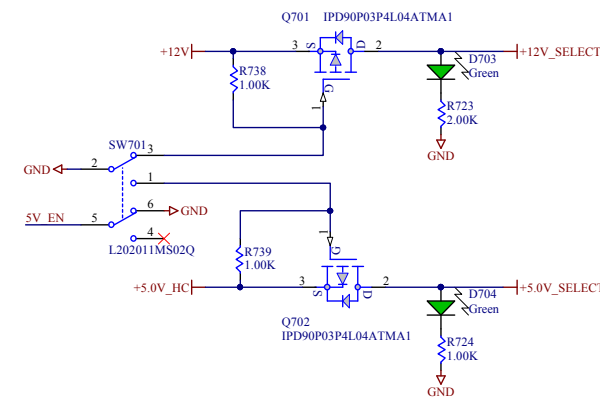
# Power Supplies



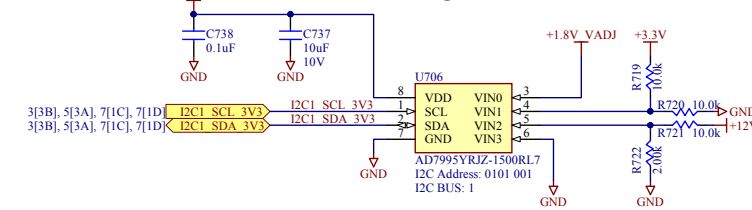
## Power Monitors



## SOM Power Selection



## Voltage Monitor



A

B

C

D

A

B

C

D

