ANLAN206

KSZ9031 Gigabit PHY Optimized Power Scheme for High Efficiency, Low-Power Consumption and Dissipation

Introduction

Even though Micrel's Gigabit PHY KSZ9031 brings many enhancements regarding power consumption, Gigabit 1000BASE-T Ethernet brings a big penalty compared to 10/100Mbps Ethernet. This increase in power consumption versus fast Ethernet must be addressed for severe-environment applications; applications that can reach more than 70°C ambient temperature around the PHY. On the other hand, some applications are not heavily constrained by ambient temperature, but rather by current/power consumption efficiency. This application note describes options available for these applications, specifically the need to either optimize or reduce power dissipation, power consumption, or size.

Depending on the KSZ9031 version used (RNX or MNX), the interface connecting the CPU MAC interface to the PHY is either GMII (Gigabit Media Independent Interface) or RGMII (Reduced Gigabit Media Independent Interface). The KSZ9031 device requires two or three power rails for a typical system design (3.3V and 1.2V, 3.3V/2.5V/1.8V for digital I/Os). The 3.3V rail powers the analog for the transceiver (AVDDH) that provides the transmit power to the transformer/RJ45. The 1.2V rail powers the analog core (AVDDL), the digital core (DVDDL), and the internal PLL (AVDD_PLL). The 1.2V rail can be built from an integrated LDO controller (using an external FET to split power dissipation) or can be supplied from an external source. The digital I/Os (DVDDH) offer a flexible solution and can be powered by 3.3V or 2.5V, or 1.8V. The CPU MAC I/O voltage to which the PHY is attached drives this. Typical power implementation is focused on a cost-optimized solution, not lowest power consumption, lowest power dissipation, nor smallest size. Figure 1 describes a typical system implementation with the KSZ9031 Gigabit PHY. We will see in this application note that changing from the typical power supply scheme can improve/optimize the system's power performance for high ambient temperature applications.

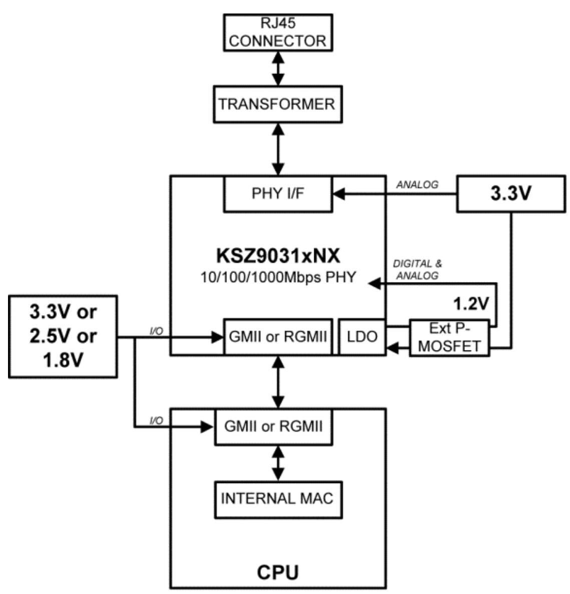

Figure 1. KSZ9031 Typical System Block Diagram

It is important to note that for applications using a greater-than 70°C ambient temperature around the PHY, an industrial grade part must be selected. Industrial grade parts are denoted with an “I” in part name. For example, KSZ9031RNXIA, KSZ9031MNXIA.

Datasheets and support documentation can be found on Micrel’s website at: www.micrel.com.

PHY Power Highlights

Table 1 illustrates the required power rails and tolerances necessary to effectively utilize the KSZ9031.

Table 1. KSZ9031 Required Power Rails

Rail	Minimum (V)	Typical (V)	Maximum (V)
Analog TX/RX Interface (AVDDH)	3.135	3.3	3.465
	2.375	2.5[1]	2.625
Digital Interface and I/Os (DVDDH)	3.135	3.3	3.465
	2.375	2.5	2.625
	1.710	1.8	1.890
Analog/Digital Core and PLL (DVDDL, AVDDL, AVDDL_PLL)	1.140	1.2	1.260

Note:

1. 2.5V AVDDH only available on C temperature version.

The KSZ9031 PHY also brings new features that provide significant enhancements of IC power consumption, such as EEE (Energy Efficient Ethernet, 802.3az). Please note that there is an erratum regarding RGMII version (KSZ9031RNX) where EEE is not supported. EEE is only supported on the GMII version, KSZ9031MNX. Because EEE highly depends on traffic through the link, a safe design rule is to size the power to sustain the worst possible case. An example of a worst-case scenario is when the PHY is in 1000Base-T full-duplex mode with 100% traffic load. Table 2 provides power consumption information on each rail for this scenario. When there is no traffic, an idle frame is sent continuously to maintain link-up state. Comparing the current consumption from the datasheet, there is little difference between 100% traffic load and no traffic load. Because traffic load is usually uncontrollable, 100% traffic load is normally used as the power consumption to design the power for the PHY.

Table 2. KSZ9031MNX (GMII) Worst Case Power Consumption in 1000Base-T Mode

Rail	Typical Consumption (mA)	Typical +20% (Process Variation) (mA)
Analog TX/RX Interface (AVDDH @ 3.3V)	68	82
Digital Interface and I/Os (DVDDH @ 3.3V)	54	65
Analog/Digital Core and PLL (DVDDL, AVDDL, AVDDL_PLL @ 1.2V)	221	265

The default power supply scheme for the KSZ9031 uses an external MOSFET to generate the 1.2V core voltage. The KSZ9031 LDO controller, as illustrated in Figure 2, drives this MOSFET internally.

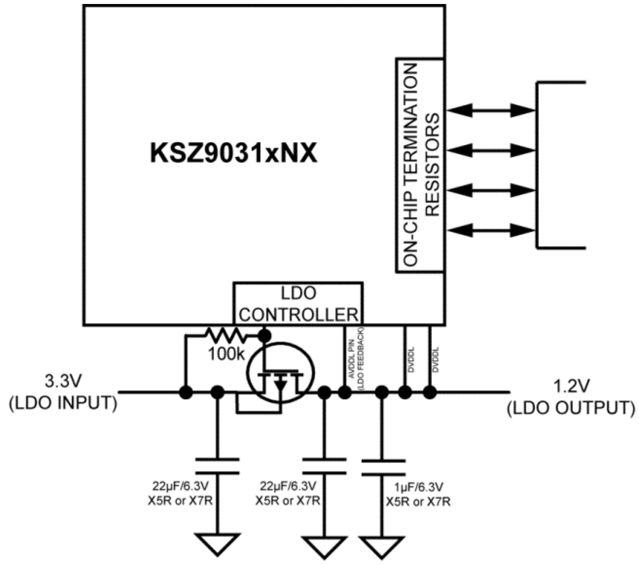

Figure 2. KSZ9031 Internal LDO Controller Driving External MOSFET

Power Architecture Performance

Solutions Overview

Figure 3 and Table 3 illustrate the distribution solutions proposed, depending on cost, size, EMI, and power efficiency/dissipation as the application constraints.

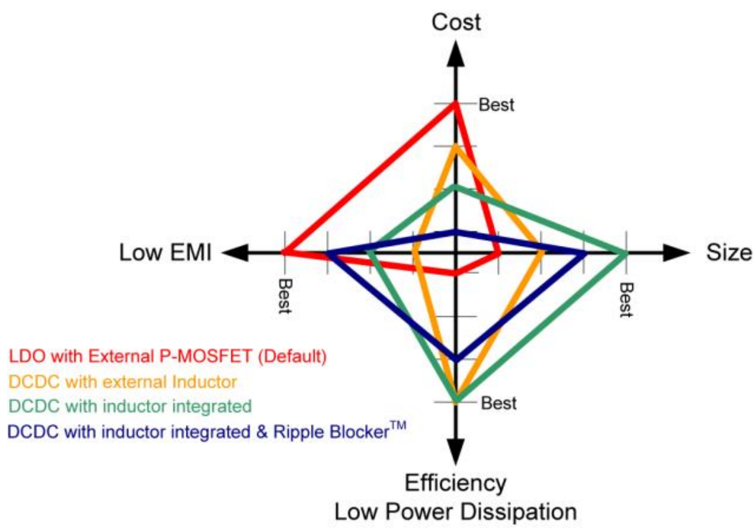

Figure 3. KSZ9031 Distribution Solutions

Table 3. KSZ9031 Distribution Solutions

Application Constraint	LDO with External FET	DC-to-DC External Inductor	DC-to-DC Internal Inductor	DC-to-DC Internal Inductor + Ripple Blocker™
Efficiency	36%	85%	82%	~80%
Size	~650mm^2	~50mm^2	~20mm^2	~30mm^2
EMI	Very Low	Caution	Low	Very Low
Cost	Very Low	Low	Medium	Medium High

See Figure 4 for step-by-step solution selection.

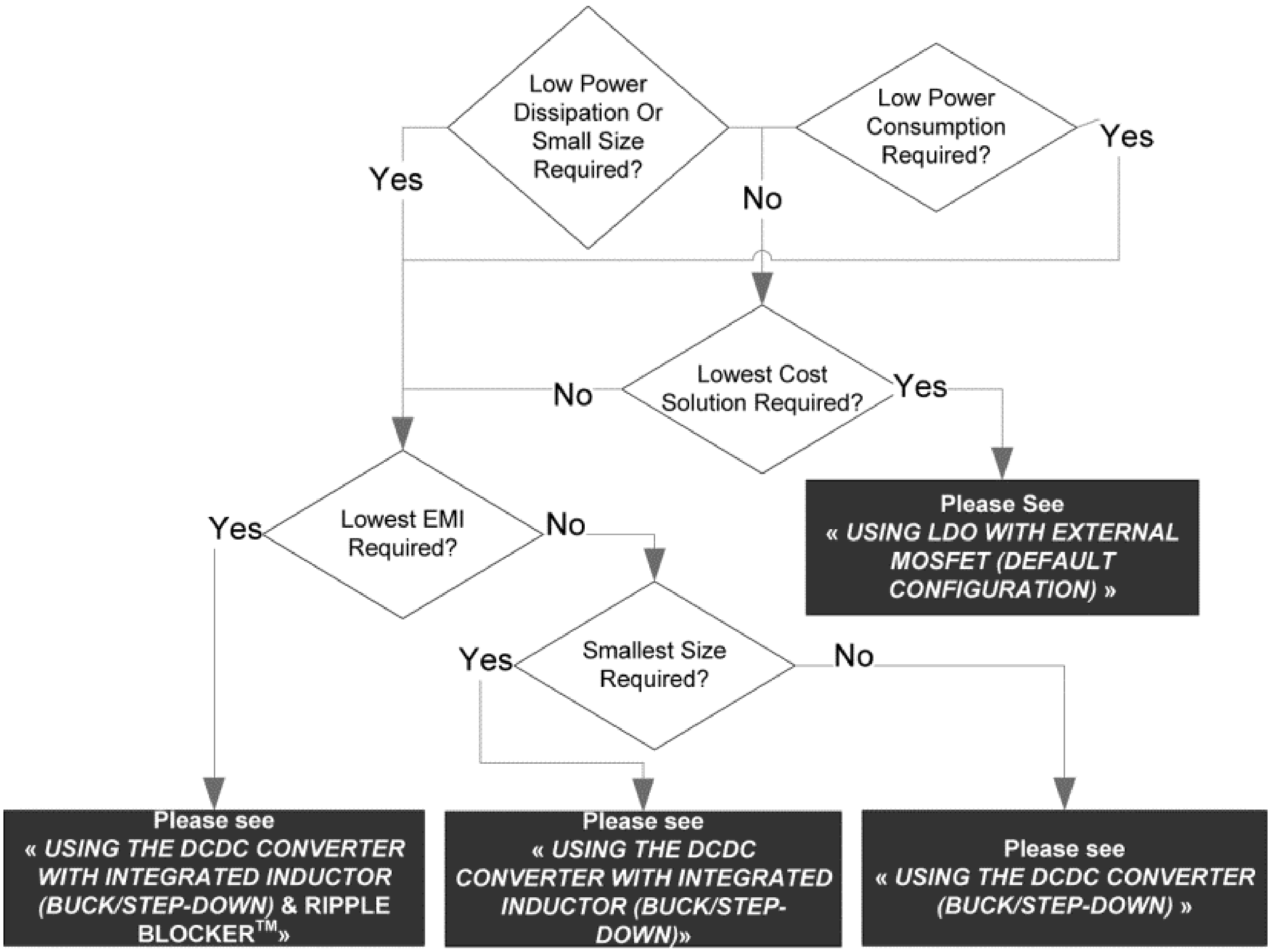

Figure 4. Design Constraint-Dependent Solution Section

Using Internal LDO with External MOSFET (Default Configuration)

Using an LDO or external MOSFET does imply a low efficiency and then high power dissipation. Equation 1 illustrates power dissipation for an LDO.

$$P_{LOSSES(MAX)} = (V_{AVDDH(MAX)} - V_{DVDDL(MIN)}) \times I_{DVDDL+AVDDL(MAX)}$$

$$P_{LOSSES(MAX)} = 0.62W \quad \text{Eq. 1}$$

The P-Channel MOSFET must dissipate 100% of this power. The maximum ambient temperature achievable, assuming the worst-case scenario, is noted in Equation 2.

$$T_{AMBIENT(MAX)} = T_{JUNCTION(MAX)} - (R\theta_{JA} \times P_{LOSSES(MAX)}) \quad \text{Eq. 2}$$

Above, $T_{JUNCTION(MAX)}$ is the maximum junction temperature of the MOSFET and $R\theta_{JA}$ is the junction to ambient thermal resistance of the MOSFET.

The MOSFET recommended in the KSZ9031 evaluation board design is the Fairchild FDT434P with a one square inch PCB heatsink. The thermal resistance is 42°C/W. In this case, the design is safe for 85°C ambient temperature around the PHY. As shown in Figure 5, the commercial temperature range (up to 70°C) allows a maximum thermal resistance θ_{JA} of 90°C/W while the industrial temperature range (up to 85°C) allows a maximum thermal resistance θ_{JA} of 65°C/W.

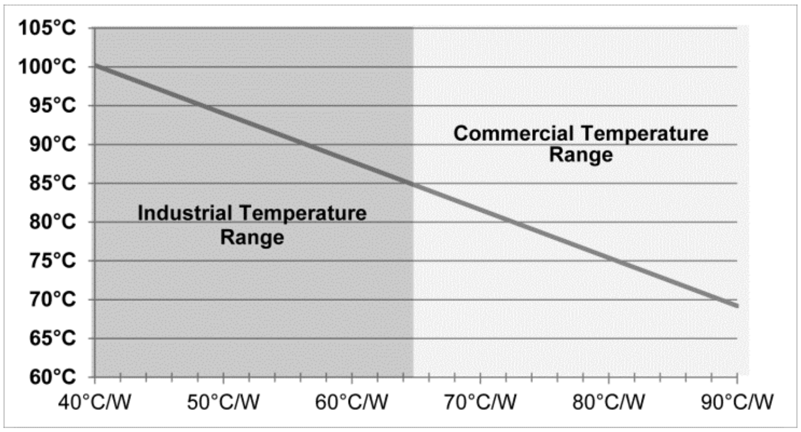

Figure 5. Maximum Ambient Temperature vs. MOSFET Thermal Resistance

From a system efficiency standpoint, the performances are not optimized. PHY sub-system efficiency is driven by 1.2V rail performances.

Power rail efficiency is given by the following formula.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \quad \text{Eq. 3}$$

For an LDO, output current is equal to input current, as shown in the following equation.

$$\eta = \frac{V_{OUT}}{V_{IN}} = \frac{1.2V}{3.3V} \cong 36\% \quad \text{Eq. 4}$$

In the default configuration, 1.2V rail efficiency is 36%, driving the need for a MOSFET with a large package and big heatsink on the PCB.

Important parameters to consider when choosing the MOSFET include:

- MOSFET package thermal resistance must comply with Figure 5Figure 4, depending on maximum ambient temperature of the application (90°C/W for commercial temperature range and 65°C/W for industrial temperature range).
- The MOSFET must allow driving the current (i.e. ≈250mA) at 1.9V VDS (LDO minimum drop-out) with a –VGS below 2.5V. Figure 6 illustrates the FDT434P example that is used in the KSZ9031 evaluation board. This parameter is particularly important to note as the MOSFET must be allowed to drive the current required with the swing available on the gate drive at the minimum LDO voltage drop. Additionally, VDS_{MIN} is (3.3V – 5%) – 1.26V ≈ 1.9V and the MOSEFT must be able to sustain approximately 250mA at 1.9V VDS.

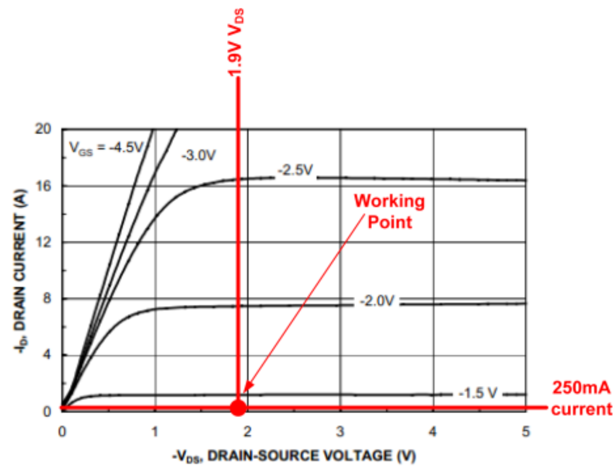

Figure 6. FDT434P Example Used in KSZ9031 Evaluation Board

- Per Figure 6, the working point shows that the MOSFET allows the voltage to drive the current at 1.9V voltage drop with a –VGS below 1.5V. FDT434P has been chosen mainly for cost.
- The input capacitance (CISS) must be below 2nF.

It is recommended to add a 100kΩ resistor between the MOSFET gate and source in order to avoid any large inrush current from 3.3V when the LDO powers up.

Other alternatives can be considered for external P-MOSFET.

Figure 7 (KSZ9031MNX) and Figure 8 (KSZ9031RNX) show the recommended power supply design for each rail. This design can be used as a baseline for decoupling capacitors. However, it is important to note that the AVDDL rail does not feature any ferrite bead when using the internal LDO controller with external MOSFET because it is used internally as the feedback sense input. A ferrite bead might degrade LDO load regulation in this case.

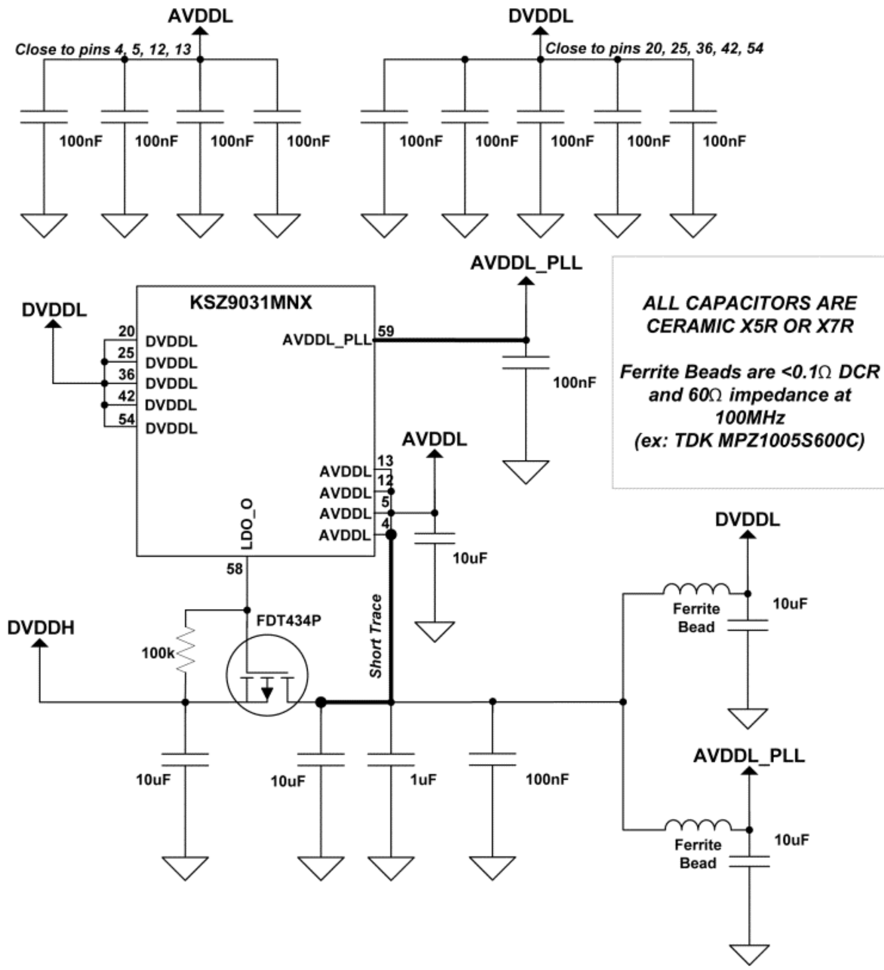

Figure 7. KSZ9031MNX Internal LDO Controller Driving an External MOSFET

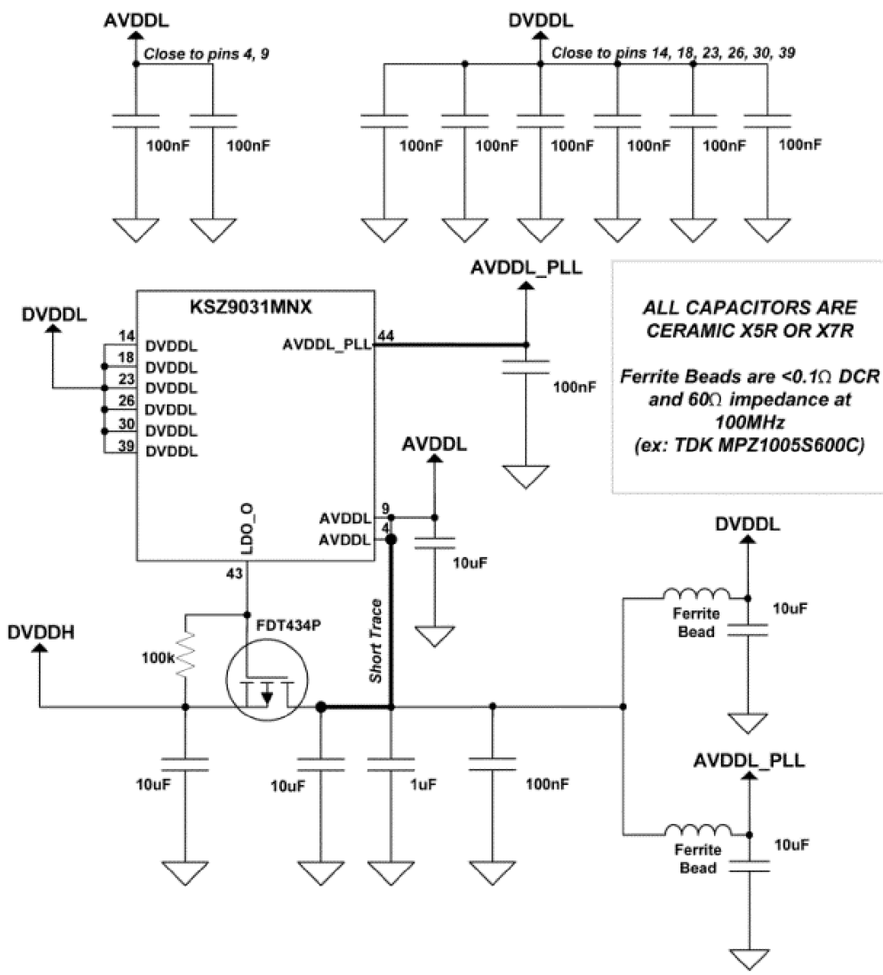

Figure 8. KSZ9031RNX Internal LDO Controller Driving an External MOSFET

Using the DC-to-DC Converter (Buck/Step-Down)

Using a DC-to-DC converter instead of an LDO (with or without external MOSFET) for the 1.2V rail will significantly enhance efficiency. This will lower current consumption and power dissipation as well. In industrial applications, ambient temperature becomes an issue. That is why it can be very important to lower all sources of heat around critical components (CPU, memory, connectivity etc.) as much as possible. Figure 3 summarizes advantages and disadvantages of such a solution.

Two options are offered depending on cost and size. These options provide much better efficiency and a smaller size compared to using an LDO with external FET.

Figure 9 shows the lowest cost solution that provides highest efficiency with a small size. In order to limit emissions, special care must be taken for layout and a shielded inductor has to be chosen. Design guidelines, reference layout and full bill of material can be found at the end of the MIC23050 datasheet: http://www.micrel.com/_PDF/mic23050.pdf.

The evaluation board document is available here:

http://www.micrel.com/_PDF/Eval-Board/mic23050_eb.pdf.

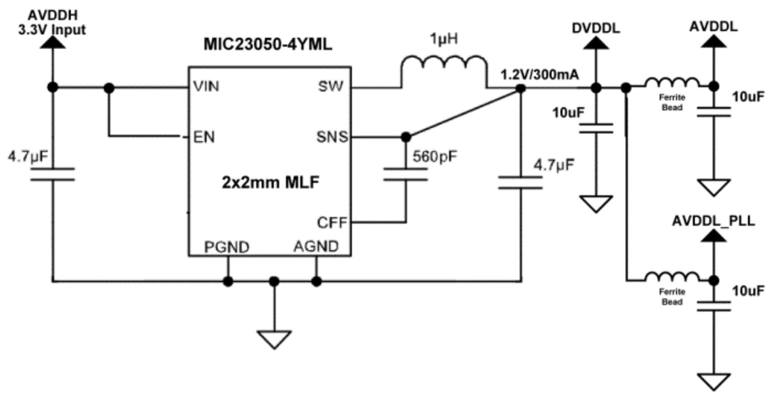

Figure 9. DC-to-DC Buck Converter with External Inductor

The MIC23050 runs at 4MHz switching frequency which provides best optimized solution in terms of size and cost without compromising on performance. 4MHz switching frequency ensures low peak current into the inductor with a low inductance value. The issue of inductor saturation is that effective inductance value drops very quickly when the magnetic circuit starts to saturate. The main consequence of this is that it leads to a high temperature rise in the inductor and overall bad performance. On one hand, a shielded inductor is usually required to reduce DC-to-DC converter emissions and to avoid any magnetic coupling between the inductor and components/traces around it. On the other hand, shielded inductors exhibit lower saturation current compared to non-shielded ones. One way to overcome the issue of low saturation current with shielded inductors is to raise the switching frequency to lower the peak current.

A high frequency, such as 4MHz, for relatively low currents (<2A), provides the best balanced solution to find small and low cost shielded inductors without significantly impacting efficiency performance. Additionally, high switching frequency allows you to space spurs in the frequency domain.

Another good point for a high switching frequency is that it allows you to use smaller input and output capacitors while also keeping very good load regulation and output ripple. The main issue with high speed digital ICs is that they require high speed load regulation during large and fast current transients. The 4MHz switching frequency and constant on-time (COT) architecture in the MIC23050 handles load transient in less than a switching cycle; that is, in less than 250ns.

Assuming the following parameters

- 4MHz switching frequency (250ns switching period)
- 1µH ±20% inductor
- 3.3V ±5% input voltage
- 1.2V ±5% output voltage

we obtain, as given by following equation, the maximum on time (maximum duty cycle).

$$T_{ON_{MAX}} = \frac{V_{OUT_{MAX}}}{V_{IN_{MIN}}} = \frac{1.26V}{3.3V - 5\%}.250ns$$

$$T_{ON_{MAX}} = 100ns \qquad \text{Eq. 5}$$

The maximum ripple current in the inductor (AC domain) is then given by the equation below.

$$DI_{L_{MAX}} = \frac{V_{IN_{MAX}} - V_{OUT_{MIN}}}{L_{MIN}} \times T_{ON_{MAX}}$$

$$DI_{L_{MAX}} = \frac{3.365V - 1.14V}{1.10\text{\^{}} - 6 - 20\%}.100ns$$

$$\Delta I_{L_{MAX}} = 278mA \qquad \text{Eq. 6}$$

The inductor minimum saturation is

$$I_{SAT_{MAX}} = (I_{LOAD_{MAX}} + \frac{\Delta IL_{MAX}}{2}) + 20\%$$

$$I_{SAT_{MAX}} = (300mA + 139mA) \times 1.20 \approx 530mA \qquad \text{Eq. 7}$$

Table 4 provides some examples of shielded inductors.

Table 4. MIC23050 Proposed Inductors

Manufacturer	Part Number	Description
TDK	TFM201210A-1R0M-T00 MLP2016S1R0MT VLS201610ET-1R0N	2mm x 1.2mm x 1mm 2mm x 1.6mm x 1mm 2mm x 1.6mm x 1mm
Coilcraft	PFL2010-102ME 0805AF-102XJR PFL1609-102ME	2.2mm x 1.4mm x 1mm 2mm x 1.2mm x 1mm 1.8mm x 1mm x 1mm
Vishay	IFSC0806AZER1R0M01	2mm x 1.6mm x 1mm
Bourns	SRU2009-1R0Y	2.8mm x 2.8mm x 0.9mm

Using the DC-to-DC Coverter with an Integrated Inductor (Buck/Step-Down)

Figure 10 shows same implementation with a DC-to-DC buck converter that integrates the inductor. The MIC33050-4YHL integrates MIC23050-4YML (see previous section) with an inductor. MIC33050 brings the same advantages as MIC23050 with lowest emissions. The package acts as a shield and switching power paths are isolated from the outside world by keeping high energy pulsed signals within the package. The performance compared to a DC-to-DC converter with external inductor is:

- Slightly lower efficiency: 82%
- Lower EMI
- Even smaller size

Design guidelines, a reference layout and bill of material can be found at the end of the MIC33050 datasheet: http://www.micrel.com/_PDF/mic33050.pdf.

Evaluation board document is available here:

http://www.micrel.com/_PDF/Eval-Board/mic33050_eb.pdf.

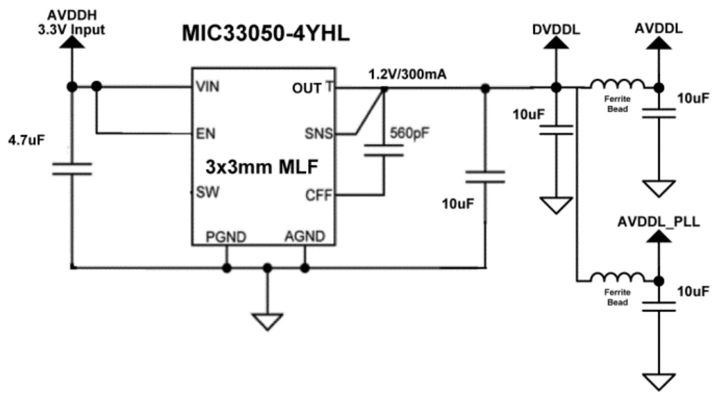

Figure 10. MIC33050 DC-to-DC Buck Converter with Integrated Inductor

Using the DC-to-DC Converter with Integrated Inductor (Buck/Step-Down) and Ripple Blocker™

When EMI and Ethernet link quality are main design drivers, it becomes critical to optimize emissions that can be transmitted through an Ethernet connection and cable. For this, it is highly recommended to design 3.3V analog power supplies in such a way that it generates low noise and low ripple. As described before, analog 3.3V is used to provide transmit power to the PHY's TX buffers (powered by AVDDH). Spurs and noise on this power rail will lead to noise and spurs on signals brought by Ethernet cable. Even though Ethernet cable is shielded in such applications, shielding quality can be vary (STP, FTP, FFTP, SFTP, SSTP). As a consequence, attenuation is not infinite and can vary greatly. Moreover, cable type is not always known when application device is plugged in an existing network.

Last but not least, analog 1.2V (AVDDL and AVDDL_PLL) are used to power the PHY's receivers (RX buffers) and internal PLL. Noise and spurs on those power rails will lead to excessive jitter on the 125MHz internal reference clock as well as less gain margin on internal receivers. This can result in a poor quality link because of excessive bit error rate.

As a result, in applications where emissions and immunity to inbound spurs are critical, it is recommended to take special care with power generation for AVDDH, AVDDL, and AVDDL_PLL.

Two types of architecture have to be considered depending on power supplies already available on the board:

- Application board does feature clean (low-noise/low ripple) 3.3V generated by an LDO. Recommended solution is described in Figure 11.
- Application board does not feature clean (low-noise/low ripple) 3.3V generated by an LDO or does feature a 3.3V generated from a switching DC-to-DC converter. Recommended solution is described in Figure 12.

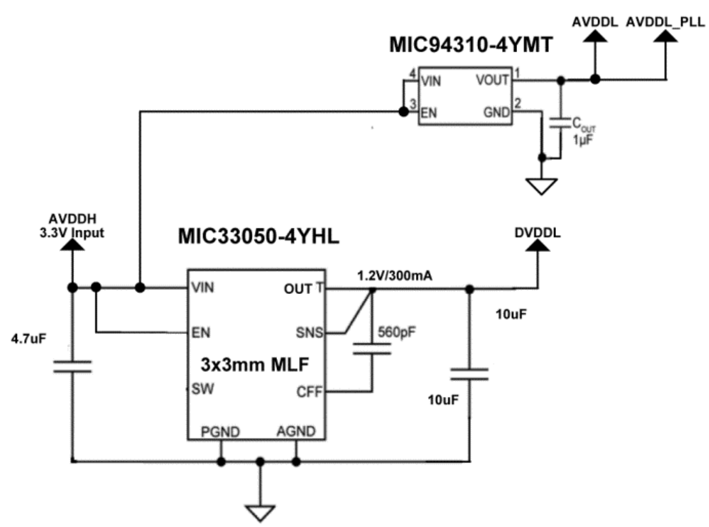

Figure 11. Low EMI/High Quality Link Solution Using Clean Analog 3.3V

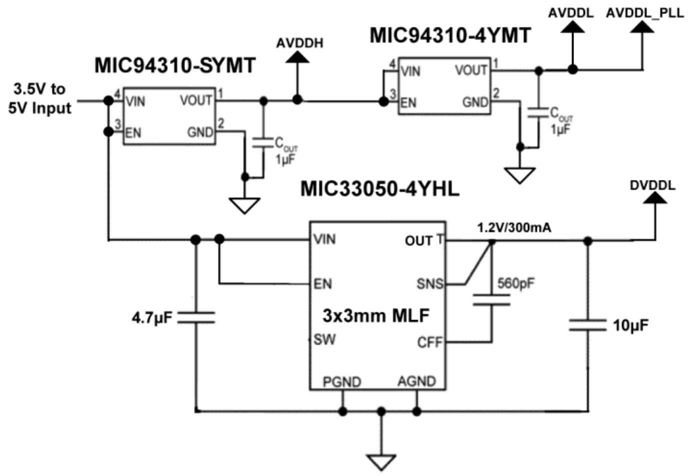

Figure 12. Low EMI/High Quality Link Solution Generating Clean Analog 3.3V

Design guidelines, reference layouts, and bills of material can be found at the end of the MIC33050 and MIC94310-4YMT/MIC94310-SYMT datasheets:

http://www.micrel.com/_PDF/mic33050.pdf.

http://www.micrel.com/_PDF/MIC94310.pdf

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