PCN# 20230801000

128 Mbit NOR Flash on:

MityDSP-L138(F)

Date: August 29, 2023

To: Purchasing Agents & Design Engineers

Dear Customer,

This is an initial announcement of a change to a product that is currently offered by Critical Link. The details of this change are on the following pages.

For questions regarding this notice, contact info@criticallink.com.

Sincerely,

Critical Link, LLC

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PCN Number: 20230801000

PCN Date: August 14, 2023

Title: 128 Mbit NOR Flash

Contact: info@criticallink.com

Phone: (315) 425-4045

EOL Date: N/A

Overview

Changes to MityDSP-L138(F) System on Modules are identified in the following sections.

1 Substitute 128 Mbit NOR flash with 256 Mbit NOR flash

1.1 Description of Change

MityDSP-L138 (F) on-SOM NOR flash was substituted with a 256Mbit part, MPN: MT25QL256ABA1EW9-0SIT in place of the original 128Mbit part, MPN: MT25QL128ABA1EW9-0SIT.

1.2 Reason for Change

This change was implemented due to availability issues with mfg P/N: MT25QL128ABA1EW9-0SIT. This is not a permanent change to the MityDSP-L138(F) family and was implemented to ensure continuity of supply chain with the SOM platform.

Moving forward the substitute flash discussed in this notice will ONLY be used on the MityDSP-L138 platforms. Any SOM part numbers with a companion FPGA will NOT be subject to this notice and will be manufactured with the original NOR flash part. Please refer to Table 2 for detail on SOM part numbers and applicability of this notice.

1.3 Anticipated Impact on Form, Fit, Function (positive / negative)

There is no impact to the Form and Fit of the MityDSP-L138 (F).

There is no impact on the hardware design, the electrical SPI bus interface has not changed.

This was expected to be a software compatible change; however, some issues were discovered, please see section 3 for known issues.

Due to this change, functionally, the memory is expanded from 128Mbits to 256Mbits. The 256 Mbit part is organized with the same-sized sectors (64 Kbytes) but increases the number of available sectors from 256 to 512. SOMs with this part are expected to be treated as if they only have 128Mbit of space. The new 256 Mbit part command set is backward compatible with the current 128 Mbit part if only the first 128 Mbit is accessed. The JEDEC Read Identification Data sequence, which is used to identify the part over the SPI bus, has changed to (0x20bb19).

Any software that reads the JEDEC identification data or tries to enable 4-bit address mode must be updated.

The following sections outline the impact for the following categories of code: First Stage Bootloader (OMAP-L138 ROM Loader), Second Stage Bootloader (UBL), Third Stage Bootloader (U-Boot), Operating System (Linux), Operating System (other), and Applications / NOR partitioning. A summary of the impact is listed in Table 1.

Table 1 SW Impact Summary

Software Category	Impact	Recommendation
First Stage / ROM Bootloader	None	No Action
Second Stage Bootloader (UBL)	None	No Action
Third Stage Bootloader(U-Boot)	Yes – New JEDEC code needed.	No action if you don't reprogram factory provided U-Boot. Otherwise, upgrade to latest U-Boot from support site.
Operating System (Linux)	Yes – New JEDEC code needed. And change to disable 4-byte address mode.	Upgrade kernel to properly identify the 256 Mbit NOR flash and disable 4-byte address mode.
Operating System (other)	Contact Supplier	Contact OS Supplier for further detail.
Applications	None	Partition sizes are the same.

1.1.1 First Stage Bootloader (OMAP-L138 ROM Loader)

OMAP-L138 ROM Loader reads the Second Stage Bootloader (the UBL) from a fixed offset in the SPI NOR device by using commands that are compatible with the 64, 128, and 256 Mbit NOR flash. The OMAP-L138 ROM Loader does not query the JEDEC ID code. There is no impact on the OMAP-L138 ROM Loader code. It will support either device without modification, if SPI NOR flash remains in 3-byte address mode.

1.1.2 Second Stage Bootloader (UBL)

The User Bootloader (UBL) reads the U-Boot application from a fixed offset in the SPI NOR flash by using commands that are compatible with the 64, 128, and 256 Mbit NOR flash. The UBL does not query the JEDEC ID code. There is no impact on the UBL code. It will support either device without modification.

1.1.3 Third Stage Bootloader (U-Boot)

The U-Boot application queries the JEDEC ID code to determine the sector format of the SPI device attached. This information is necessary to support erase/write operations. The sector information is stored in a compiled-in lookup table keyed by the JEDEC ID. The U-Boot application delivered on older modules or compiled prior to 2022-Jun-23 does not contain a table entry for the 256 Mbit device. The U-Boot code, available on our public git

repository, includes the necessary patches to support the 256 Mbit device. The U-Boot application delivered on modules has been updated to include the patch.

There is no impact for customers that use the factory installed U-Boot for their end applications.

Customers that install their own version of U-Boot must incorporate the following patch outlined by the following commit:

cf500735a984: Add support for Micron versions of SPI NOR flash up to 2Gb

1.1.4 Operating System (Linux)

Prior to 2017-12-25, the officially supported versions of the Linux kernel by Critical Link (versions 2.6.34 and 3.2) hardcoded the SPI NOR FLASH ID to the 64 Mbit device by defining the "type" field in the SPI flash configuration data in the board-mityomapl138.c file. Customers using these versions of the kernel with modules having the 256 Mbit device installed will only be able to access the first 64 Mbit of flash area (only because the sector sizes and command sets are compatible between the 64, 128, and 256 Mbit devices), and the kernel will not correctly identify the device during the boot process.

Critical Link has included a patch set to introduce the new 256 Mbit part data in the kernel lookup table, as well as instruct the kernel to use the JEDEC ID code from the part to determine which device is installed and support it appropriately. The patches are available on the Critical Link support site.

The 3.2 kernel and newer, use the 4-Byte NOR address mode to enable access to the upper portion of the NOR flash. This causes issues with reset/reboot as mentioned in section 3.1. Solutions for this are not introduced until the 4.10 kernel in the form of new stateless 4-byte read/write commands, however since backporting all these changes may lead to unforeseen bugs, our current solution is to limit the flash to 128 Mbit 3-byte addressing.

Customers using the 2.6 kernel should not need to update as it doesn't support the 4-byte addressing mode.

Customers with newer kernels need to update their kernel version to include these patches in order to correctly identify the device and leave the NOR flash in 3-byte addressing mode:

mitydsp-linux-v3.2 Branch: NEED TO UPDATE
e752a55281883c9ea1d688dd0db4404c1a97839a: Auto-probe the SPI NOR flash type using JEDEC ID.
27a97bd689bb76496658d0c47a98eee93ab2a672: Add micron JEDEC IDs and block sizes to support newer NOR FLASH devices.
22af66aae84: mtd: spinor: HACK: Disable 4byte spinor mode

1.1.5 Operating System (other)

Customers that use operating system software such as embedded windows or QNX should contact their OS provider for details. Customers developing Starter ware or writing bare metal applications and are using the SPI

NOR flash device must assess the impact, if any, of the device change on their application software. Contact Critical Link if further assistance is required.

1.1.6 **Applications / NOR Partitioning**

Because both devices use 64 Kbyte sectors, there is no need to alter the NOR partitioning on a working / fielded application. No impact is anticipated on application software.

1.4 Anticipated Impact on Quality or Reliability (positive / negative)

There is no impact to Quality or Reliability.

2 Products Affected

Details regarding the full revision history can be located in the MityDSP-L138 Revision History section on the Critical Link support site.
https://support.criticallink.com/redmine/projects/arm9-platforms/wiki/Module_Product_Change_Notifications

*- custom P/N

Table 2 Products Affected

Model Number	Subject to Substitution moving forward	Comment
L138-FI-336-RL	No	
L138-FI-325-RC	No	
L138-FG-326-RC	No	
L138-FG-325-RC	No	
L138-DI-325-RI	No	
L138-DG-325-RI	No	
L138-DI-336-RI	No	
L138-FM-336-RL	No	
L138-FJ-326-RC	No	One time substitution made on Lot Code 23-01-01
L138-DJ-325-RI	No	
L138-DM-336-RI	No	
L138-DH-336-RI	No	
L138-FI-336-RL	No	
L138-FI-325-RC	No	
L138-FI-326-RC	No	One time substitution made on Lot Code 22-10-06
80-001110RL-6*	No	
L138-FX-325-RC-E	Yes	Substituted on Lot Code 22-10-05. Eligible for substitution as required in the future.
L138-FX-325-RC	Yes	Substituted on Lot Codes 22-08-16 and 22-10-04. Eligible for substitution as required in the future.
L138-DX-325-RI	Yes	Eligible for substitution as required in the future.

3 Appendix:

3.1 4-Byte NOR Address Mode and Reset/Reboot Issue

Historically NOR flash has used a 3-byte address mode to address data. With the introduction of NOR flash with over 16MiB of storage, manufacturers added a special command set to switch to a 4-byte address mode. This required all READ/WRITE commands to pass an additional byte for addressing and would fail if the smaller 3-byte address was passed. This solution is stateful: it changes the internal state of the memory.

Hence, when the CPU is reset but not the flash, many bootloaders are not aware of this internal state change at the memory side and don't know how to handle this. In these cases, the bootloader still sends one Fast Read op

code followed by a 3-byte address. So, the bootloader does not read data from the SPI flash memory and boot fails, appearing to hang indefinitely.

Historical related discussions:

http://lists.infradead.org/pipermail/linux-mtd/2013-March/046343.html
[PATCH 1/3] mtd: m25p80: utilize dedicated 4-byte addressing commands

http://lists.infradead.org/pipermail/barebox/2014-September/020682.html
[RFC] MTD m25p80 3-byte addressing and boot problem

https://patchwork.ozlabs.org/project/linux-mtd/patch/20180727183313.137943-1-computersforpeace@gmail.com/#1965591
mtd: spi-nor: only apply reset hacks to broken hardware.

3.2 MityDSP-L138 Configuration Block Settings

64Kbyte of the on-SOM NOR flash is reserved to store configuration settings for enabling peripherals such as MMC, LCD, UARTs etc. Due to the 4-byte addressing issue mentioned above it is possible that these configuration settings may not be read correctly and may cause peripherals like the LCD interface for example to not be configured properly. This specific error only applies to our 3.2 kernel. The older and newer kernels are not affected.

If you experience any similar issues, please try the updates and associated instructions listed in this PCN. If you still require further support please contact Critical Link, LLC.

4 Document Revision History

Date	Version	Change Description
14-Aug-2023	1.0	Initial Version
1-Sep-2023	2.0	Updates to Table 2 Products Affected