# Overview

This document will detail the register interface to the L138 port of the Timing Generator core. In general, the register map is stretched for high order bits on odd addresses with the register being latched after writing to the even register (low order bits).

# Map

|  |  |  |
| --- | --- | --- |
| Address | R/W? | Meaning |
| 0x0 | R | Version Register |
| 0x1 | R/W | Status Register High |
| 0x2 | R/W | Status Register Low |
| 0x3 | R/W | Payload Override Enable |
| 0x4 | R/W | Payload Override Value |
| 0x5 | R/W | Interrupt Enable High |
| 0x6 | R/W | Interrupt Enable Low |
| 0x7 | R/W | Interrupt Status High |
| 0x8 | R/W | Interrupt Status Low |
| 0x9 | R/W | Instruction Write Address High |
| 0xA | R/W | Instruction Write Address Low |
| 0xB | R/W | Read/Write Data High |
| 0xC | R/W | Read/Write Data Low |
| 0xD | R | Instruction RAM depth High |
| 0xE | R | Instruction RAM depth Low |
| 0xF | W | Alternate Jump Table Write |

## Version

Accesses to this register follow the standard L138 version core access

## Status Register

A 32-bit register for status/control of the timing generator core

## Payload Override Enable

16 bit enable for the 16 payload bits. When a 1 is written to a specific bit, the corresponding value from payload override is used on the output instead of that which is in the microcode instruction.

## Payload Override Value

16-bit vector of override bits; these bits are used instead of the microcode instruction payload when the corresponding enable bit is set high.

## Interrupt Enable

Write a 1 to enable interrupts for a particular bit of the payload.

## Interrupt Status

Write a 1 to the particular bit to clear the interrupt.

## Instruction Write Address

Set the location in the instruction block RAM to begin writing instructions to.

## Read/Write Data

Reads back the current instruction loaded at the Instruction Write Address location in the Instruction block RAM.

Write a data word to the location currently pointed at by the Instruction Write Address. Writing to this register will auto-increment the write address making it possible to write a timing program by setting a start address and then only writing this register.

## Instruction RAM Depth

Reads back the instruction RAM depth; this is the number of 32-bit instructions that can be written.

## Alternate Jump Table Write

A write only register; writes to the alternate jump table. The bit map is as follows:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 15 | 14 | 13:12 | 11:9(8) | 9(8):0 |
| Jump Valid | Reserved | Jump Write Address | Reserved | Jump Address |

Specify if the jump is valid at a particular location in the jump table.

The Jump Write Address is the address in the jump table to write to.

Bits 9 or 8 (depending on the size of instruction RAM generated) downto 0 correspond to the instruction RAM address to jump to.

# I/O

## Reading

Reading is done 16 bits at a time on the registers. The contents are valid immediately. Reading does not reflect intermediate writes on registers which have two halves. That is, if you write just to the high bits of interrupt enable, then read back the register, the high bits that were written have not been latched because the low order register was not written to yet.

## Writing

Writes are always performed in two steps for 32-bit registers. The first write to an odd address latches the high order data into a temporary register. The second write to an even address will then latch the entire contents into the final register. Some registers are only 16 bits wide. Specifically, “Payload Override Enable and Value,” and “Alternate Jump Table Write” are 16 bits and will be written to immediately.